highstreet
PTP Hardware Assist

Product Flyer

OVERVIEW

The Precision Time Protocol (PTP) acc. to IEEE standard 1588^{TM}-2008 enables the distribution of frequency and time-of-day over packet switched networks with unprecedented accuracy. Besides the quality of the used oscillators and the capability of the servo-mechanism averaging the variation of the timing packets' transfer delay, the performance of PTP strongly depends on the precision of delay measurement and time-stamping. Only a hardware-based solution like the highstreet PTP Hardware Assist can provide the accuracy required for the synchronization of e.g. radio access and power distribution networks.

The highstreet PTP Hardware Assist is an IP-Core that is placed on top of the physical interfaces of an FPGA where it timestamps the ingress and the egress of PTP event messages. Additionally, it measures the packets' residence time in the device and performs the necessary corrections. It can determine the path delay to a peer node, correct any asymmetries, and then add it to the timestamp of the timing packets. By enabling one or more of these features, the highstreet PTP Hardware Assist is deployable in ordinary, boundary, and transparent PTP clocks.

Although being developed for operation on top of Xilinx' Embedded Tri-Mode Ethernet MAC and RocketIO Multi-Gigabit Transceiver, on request, the highstreet PTP Hardware Assist can easily be adapted to other physical interfaces. If so desired, the VHDL source code of the highstreet PTP Hardware Assist is reusable for the design of ASICs.
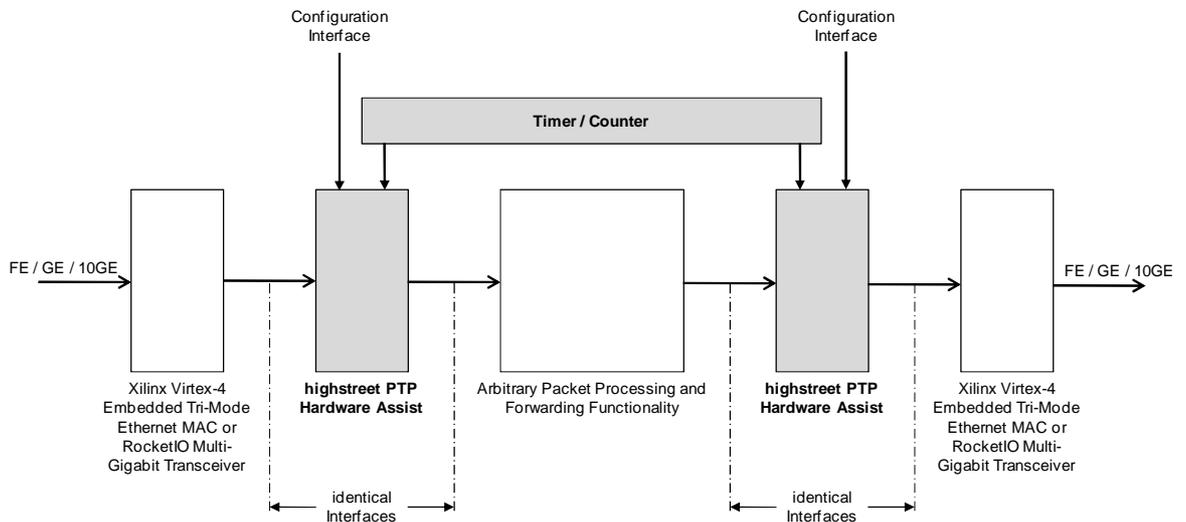
ARCHITECTURE

The highstreet PTP Hardware Assist modules are inserted between the physical interfaces of a device and an arbitrary packet processing and forwarding entity. Since they present the same interface as the physical interface, other modules may remain unchanged. A timer respectively counter provides accurate timing information to the highstreet PTP Hardware Assist modules. Via a dedicated configuration interface, the PTP Hardware Assist is configurable for operation on a PTP ordinary, boundary, or transparent clock.

On a PTP ordinary clock, i.e. grandmaster or slave clock, the highstreet PTP Hardware Assist module time-stamps Sync and Delay_Req messages. In peer-to-peer mode, the timestamp is optionally corrected with measured path delay and path delay asymmetry.

The behaviour on a boundary clock is very much the same, only that there are one PTP slave port and one or more PTP master ports.

On a PTP end-to-end transparent clock, the highstreet PTP Hardware Assist modules measure the residence time of the PTP event messages and correct the timestamps accordingly. Known path delay asymmetries are optionally considered.

On a PTP peer-to-peer transparent clock the path delay to the peer clock is measured and used for correcting the timestamps of the PTP event messages.

Architecture of the highstreet PTP Hardware Assist

FEATURES

The main features of the highstreet PTP Hardware Assist are the

- Time-stamping of the PTP event messages at ingress and egress,

- Measurement of the residence time and corresponding timestamp correction,

- Consideration of path delay and path delay asymmetry and corresponding correction of the timestamp,

- Optional measurement of path delay in peer-to-peer mode,

- Optional correction of local clock's rate deviation.

Additional features can be added on short notice.

PRODUCT-RELATED SERVICES

highstreet technologies offers a series of services related to the highstreet PTP Hardware Assist, amongst the most interesting are the

- Porting and testing of the PTP Hardware Assist to other FPGA than Xilinx' Virtex-4,

- Adaptation to other physical interfaces than the Xilinx Embedded Tri-Mode Ethernet MAC and the RocketIO Multi-Gigabit Transceiver,

- Adaptation of the configuration interface to specific needs,

- Addition of functionality as required,

- Support for the integration of the VHDL source code into ASIC designs.